SD

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,959	06/20/2003	Afzal M. Malik	SC12865TH	6580

23125 7590 01/04/2005

FREESCALE SEMICONDUCTOR, INC.
LAW DEPARTMENT
7700 WEST PARMER LANE MD:TX32/PL02
AUSTIN, TX 78729

EXAMINER	
CHACE, CHRISTIAN	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 01/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,959	MALIK ET AL.	
	Examiner	Art Unit	
	Christian P. Chace	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-23* is/are rejected.

7)☒ Claim(s) *7 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/20/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Information Disclosure Statement

IDS submitted 20 June 2003 has been considered by examiner. A signed and initialed copy is attached hereto.

Specification

The disclosure is objected to because of the following informalities:

In lines 25-27 of page 6 of the instant specification, the same burst line (36) appears to have been erroneously recited – should the second citation in line 27 be burst line 38, for example?

In line 15 of page 8 of the instant specification, an "Address Tag Field" is recited. Line 21 of the same page recites, "The Tag Field." Are these the same tag fields?

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 11-12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 11 recites, "determining a number of data requests to a memory addressed by the read request based on a bus width of a bus interfacing with the memory." The specification does not enable one of ordinary skill in the art to perform

this determination. Claim 12 depends upon the instant claim and is rejected for at least the reason cited supra with respect to same.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 11 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As discussed supra, claim 11 recites, "determining a number of data requests to a memory addressed by the read request based on a bus width of a bus interfacing with the memory." It is unclear whether this is determining a burst length or some other procedure. It appears it is not bursting because the second limitation of claim 11 could be interpreted a determining the burst length as well.

For the purposes of examination, however, examiner has interpreted the first limitation of claim 11 to be the determination of the burst length, and the second limitation to be the determination of the "data size," or prefetch size, as will be discussed below. Claim 12 depends upon the instant claim and is rejected for at least the reason cited supra with respect to same.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6, 8-16, and 19-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Peters et al (US Patent 6,636,927).

With respect to independent claim 1, a method for configuring a prefetch buffer, comprising receiving a read request from a master, and, in response to the read request, selectively modifying a "line size" (data size) of at least a portion of the prefetch buffer based on an attribute of the read request is disclosed in the abstract in last ten lines, specifically.

With respect to claim 2, the attribute of the read request comprising a master identifier corresponding to the master is disclosed in the abstract as a prefetch control register being associated with the a master device, the prefetch control register being associated with a particular master device inherently identifies the master.

With respect to claim 3, selectively modifying the line size being "based on" a second attribute of the read request, wherein the second attribute comprises a data size is disclosed in the abstract as the prefetch size.

With respect to claim 4, the read request resulting in a miss in the prefetch buffer is disclosed in column 4, lines 38-40. When the prefetch buffer does not have the data, the data is not transferred from it, which is, by definition, a miss.

With respect to claim 5, the prefetch buffer including a plurality of lines, each of the lines having a "corresponding one" of "status fields," is disclosed in column 3, lines 50-57. The prefetch control registers "correspond" to the buffers that have lines.

With respect to claim 6, selecting at least a portion of the plurality of lines as a "replacement entry" within the prefetch buffer based on the status fields of the prefetch buffer is disclosed in column 4, lines 41-47.

With respect to claims 8 and 21, selectively modifying the line size comprising selectively modifying a line size of the replacement entry is disclosed in column 4, lines 41-47. If the buffer has different segments, each assigned to different masters, and, as discussed supra, each master has it's own respective line size, then the line size of the "replacement entry" will be different than the original.

With respect to claims 9 and 16, selectively modifying the line size of the replacement entry comprising selectively modifying a status field corresponding to the replacement entry is disclosed in column 7, lines 29-31 as the register is programmable.

With respect to claim 10, selectively modifying the status field corresponding to the replacement entry being based on the attribute of the read request, the attribute comprising a data size is disclosed in column 8, line 42, for example, as the prefetch size.

With respect to claim 11, determining a number of data requests to a memory addressed by the read request based a bus width of a bus interfacing with a memory is disclosed as bursts in column 2, lines 31-33, where the data requests are single units of data. Bursts inherently have a length associated with them, by definition.

Determining a size of the data requests to the memory "based on" the data size corresponding to the read request and on the status field of the replacement entry I disclosed in column 4, lines 42-47 as "segmented buffers." Also, the data size could be interpreted, as supra, as the "prefetch size."

With respect to claim 12, generating data requests to the memory and storing data from the memory into the replacement entry of the prefetch buffer is disclosed in column 3, lines 50-57.

With respect to claim 13, generating at least one data request to a memory addressed by the read request and storing data from the memory into the replacement entry of the prefetch buffer is disclosed in column 3, lines 50-57. Examiner notes that claims 12 and 13 merely describe how a buffer works, by definition.

With respect to independent claim 14, a method for configuring a prefetch buffer is disclosed in the abstract.

Receiving a read request to a memory from a requesting master, the read request having a "corresponding " data size (prefetch size) and burst length (bursting is disclosed in column 2, line 33 and inherently has a length as discussed supra, is disclosed in column 3, lines 37-42 and 50-57.

Providing a prefetch buffer reconfiguration indicator "based on" the data size and the burst length is disclosed in column 3, lines 37-42.

Selecting a replacement entry within the prefetch buffer and based on the prefetch buffer reconfiguration indicator, selectively modifying line size of the replacement entry and storing the data fetched from the memory in the replacement

entry is disclosed in column 4, lines 41-47. Inherently, buffers are filled and emptied as needed – otherwise, once they filled, they would no longer be useful if the data in them is no longer needed by the master. Accordingly, the registers are programmable for future prefetches.

With respect to claim 15, the prefetch buffer reconfiguration indicator being "based on" the data size (prefetch size), the burst length (discussed supra), and a master identifier corresponding to the requesting master (also discussed supra) is disclosed in column 3, lines 37-42 as the prefetch control register.

With respect to claim 19, generating at least one data fetch request to the memory wherein the at least one data fetch request is "based on" a bus width corresponding to a memory is disclosed in figure 5, #506. Data fetches are inherently "based on" a bus width in that only s much data can be fetched at a time, depending on the size (width) of the bus carrying it.

With respect to independent claim 20, a data processing system is disclosed in the title.

A master is disclosed in figure 2, #212, for example.

A memory is disclosed in figure 2, #230, for example.

A prefetch buffer, coupled to the master and the memory, the prefetch buffer having a plurality of lines is disclosed in figure 3, #304 and discussed in the abstract.

Prefetch control circuitry coupled to the prefetch buffer, the prefetch control circuitry, in response to a read request from the master, selectively modifying a line size (prefetch size) of at least a portion of the prefetch buffer is disclosed in figure 3, #302,

which is further disclosed in figure 4 as #402, and discussed in the abstract, for example.

With respect to claim 22, the prefetch control circuitry receiving a data size indicator and a burst length indicator from a master and selectively modifying the line size (prefetch size) of the replacement entry "based on" the data size indicator and the burst length indicator is disclosed in column 2, line 33. The indicators are inherent in that in peters et al, a discussed supra, the prefetch size and burst size are both indicated. Therefore, there must be an indicator of some sort to do the indicating, as a computer must be told what to do.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peters et al (cited supra) in view of Hicks et al (US Patent #6,085,291).

With respect to claims 17 and 18, Peters et al disclose the limitations of the claims upon which the instant claims depend. Peters et al disclose a status field in the prefetch registers.

The difference between Peters et al and the instant claims, however, are the explicit recitations of the status field comprising an address tag field, wherein selectively modifying the at least one status field comprises selectively modifying the address tag

field as well as selecting the replacement entry within the prefetch buffer comprising checking a valid bit within the status field of the prefetch buffer.

However, Hicks et al disclose the address tag field and modification of same in figure 3, "ADR" as well as in figure 5, "LINE ADR." In addition, figure 5 shows the valid bit being a part of the stream address buffer.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, having the teachings of Peters et al and Hicks et al before him/her, to utilize the address tag field and valid bits of Hicks et al in the status field of Peters et al, because the address bit can be used to allocate the corresponding data into the buffer, as discussed by Hicks et al in column 6, lines 43-45, for example, as well as use of the valid bit in the status being used to indicate whether the stream (data) is allocated, as discussed by Hicks et al in column 6, line 50, for example.

Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peters et al (cited supra).

Peters et al disclose the limitations of the claims upon which the instant claim depends.

The difference between Peters et al and the instant claim language is the explicit recitation that the prefetch buffer itself contains the status fields, each of the lines having a corresponding one of the status fields. Examiner notes that this claim language does not require every line to have it's own, separate, status field; rather, that each line corresponds to one of the status fields, which is anticipated by Peters et al

and their prefetch registers. However, those registers and status fields actually being in the buffer is not taught by Peters et al.

However, it is well known by those of ordinary skill in the art that any operation performed by hardware can be performed by software. The decision to put certain functions in hardware and others in software is based on such factors as cost, speed, reliability, and frequency of expected changes. Designers with different goals may, and often do, make different decisions. The examiner takes OFFICIAL NOTICE of this teaching.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention, having the teachings of Peters et al before him/her, to use the hardware technique of Peters et al instead of the software technique of the instantly claimed invention, for the reasons discussed supra, as made hackneyed in the state of the art.

Allowable Subject Matter

Claims 7 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

With respect to claims 7 an 24, the claimed combination of fields is not taught or suggested by the cited prior art of record, nor is there any motivation to combine the fields that are actually disclosed, such as the valid field and address tag, as discussed

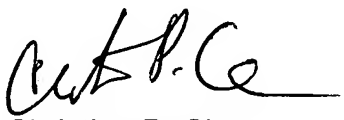
supra, with the additionally claimed fields of the instant claims, such as, e.g., the "used" field.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian P. Chace whose telephone number is 571.272.4190. The examiner can normally be reached on MAXI FLEX.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571.272.4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Christian P. Chace
Examiner
Art Unit 2187